



## Supplementary Materials for

### **Tailoring Electrical Transport Across Grain Boundaries in Polycrystalline Graphene**

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## Materials and Methods

### Synthesis of graphene with various domain size $D$ :

All graphene is grown on 25  $\mu\text{m}$  thick copper foil in a custom hot-wall quartz tube furnace at  $\approx 2$  Torr pressure using the process reported by Li *et al.* (2).

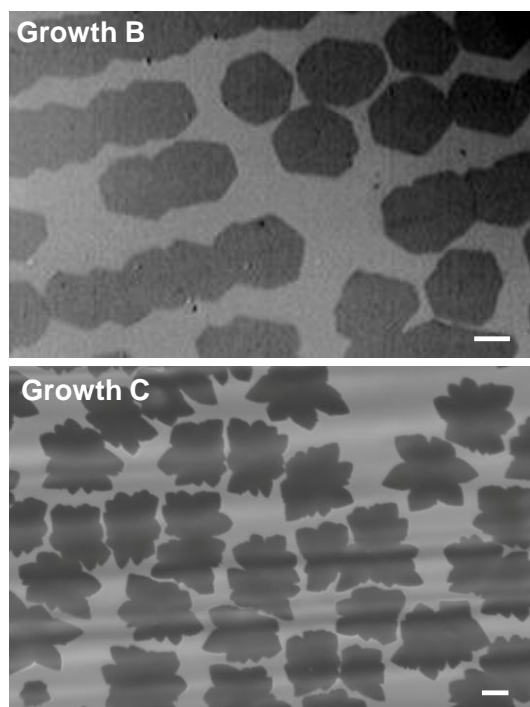
Growth A ( $D \approx 1 \mu\text{m}$ ): Copper substrates were heated to the reaction temperature of 1000  $^{\circ}\text{C}$  in a hydrogen environment ( $\text{H}_2$ : 100 sccm). After annealing for one hour, methane ( $\text{CH}_4$ : 6 sccm) was introduced. Following a 10 minute growth stage, the chamber was slowly cooled to room temperature.

Growth B ( $D \approx 10 \mu\text{m}$ ): Copper is heated to 1050  $^{\circ}\text{C}$  in a hydrogen environment ( $\text{H}_2$ : 300 sccm) and annealed for 30 minutes. Methane ( $\text{CH}_4$ : 0.8 sccm) is introduced for 30 minutes for partial growth (Fig. S1, top) and 90 minutes for complete coverage. The furnace is subsequently cooled.

Growth C ( $D \approx 50 \mu\text{m}$ ): After Li *et al.* (14), a closed "pocket" made of copper foil was heated between 980-1000  $^{\circ}\text{C}$  in a hydrogen environment ( $\text{H}_2$ : 60-120 sccm) and annealed up to 3 hours. Methane ( $\text{CH}_4$ : 1 sccm) is introduced for 90 minutes for partial growth (Fig. S1, bottom) and  $\approx 3$  hours for complete coverage, after which the furnace is cooled.

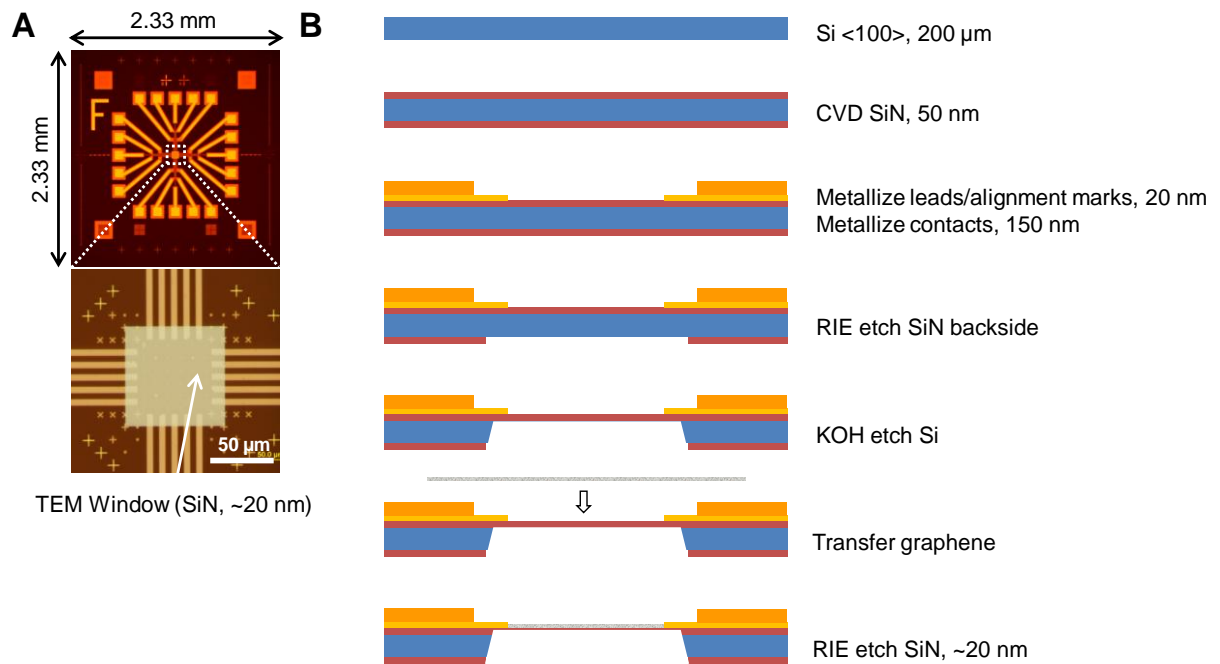
### Fabrication of transmission electron microscopy chip compatible with electrical measurements:

Here, we describe the fabrication of transmission electron microscopy (TEM) chips that are compatible with electron-beam lithography and electrical measurements. A completed chip is shown in figure S2 (A). It is 2.33 mm wide on each side, 200  $\mu\text{m}$  thick, and fits standard holders. In the center is a fully suspended, silicon nitride (SiN) TEM window (80x80  $\mu\text{m}$ , 20 nm thickness) with metalized alignment marks. On the periphery are large electrical leads and contacts. The chips are fabricated on the wafer scale using optical lithography and cleaved individually at the end. A schematic of the process flow is shown in figure S2 (B). First, we grow 50 nm of low stress SiN on 200  $\mu\text{m}$  thick silicon (Si)  $\langle 100 \rangle$  wafers. In two separate lithography steps we pattern and metalize alignment marks and electrical leads close to the TEM window (20 nm Cr/Au) as well as contact pads on the chip periphery (150 nm Cr/Au). Next, we pattern and etch large SiN windows on the backside of the chip using reactive ion etching (RIE) to allow for KOH etching of the Si substrate underlying the TEM window. After transferring graphene, the SiN TEM window is further thinned from the back to  $\approx 20$  nm with RIE.



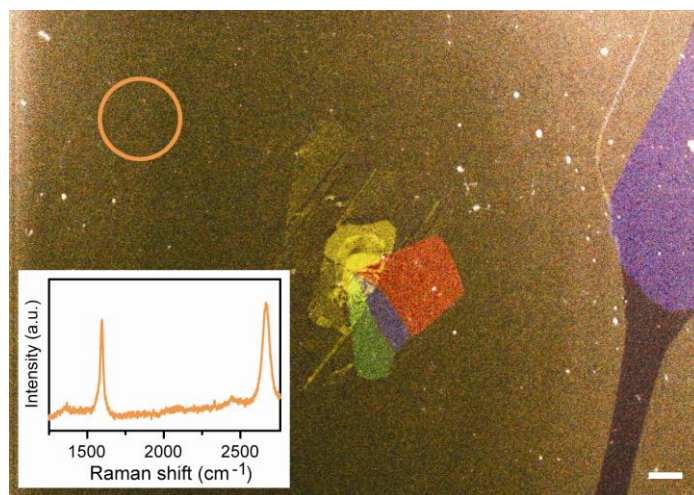
**Fig. S1**

Top: optical image of polygon graphene islands from growth B transferred onto SiO<sub>2</sub>/Si. Bottom: optical image of flowered graphene islands from growth C on copper foil. Scale bars: 10 μm.



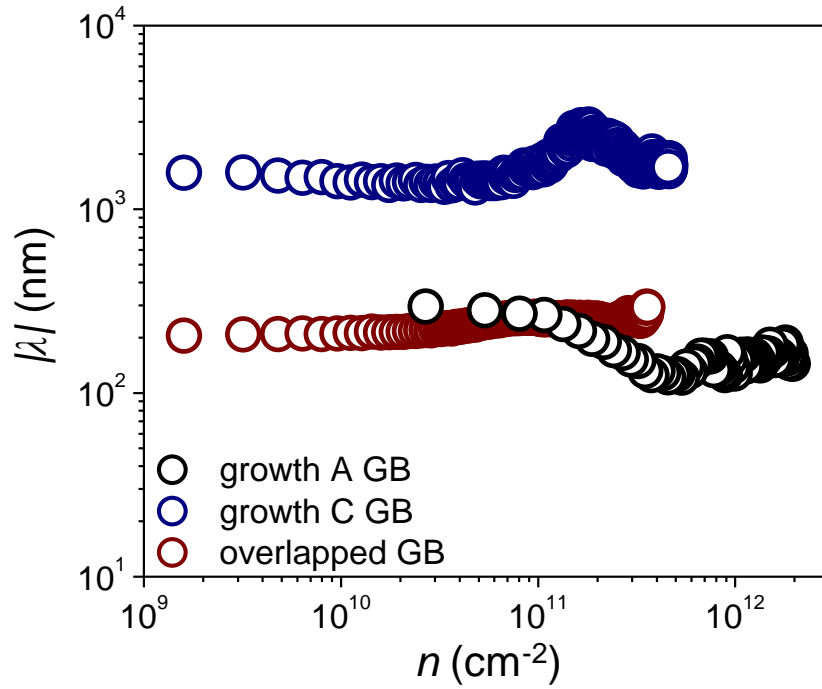
**Fig. S2**

(A) Optical images of completed TEM chip compatible with e-beam lithography and electrical measurements. (B) Schematic outlining fabrication procedure: 1) Grow 50 nm of SiN on 200  $\mu\text{m}$  thickness Si wafer. 2) Metallize electrical contacts and leads. 3) RIE etch SiN windows on backside for 4) KOH etch of Si. After transferring graphene, 5) thin SiN TEM window to  $\approx 20$  nm from backside with RIE.



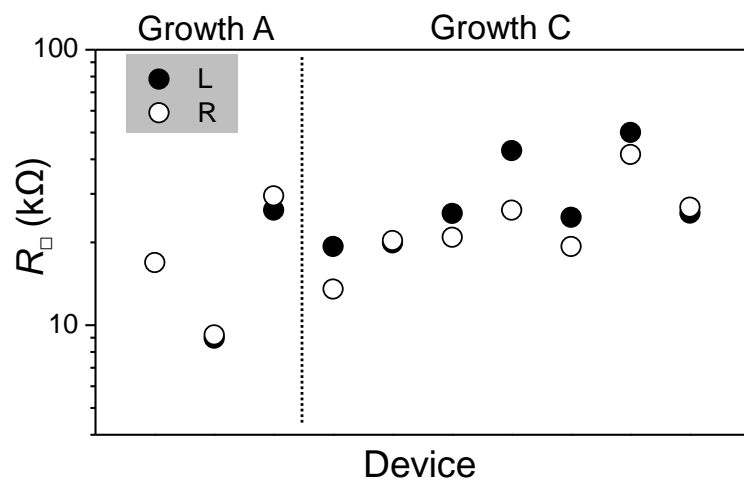
**Fig. S3**

Micro-Raman spectrum (inset) of graphene taken after dark-field TEM imaging (main panel). Small D peak shows minimal radiation damage in contrast with (26) and (27). Raman location is indicated by circle. Scale bar: 1  $\mu\text{m}$ .



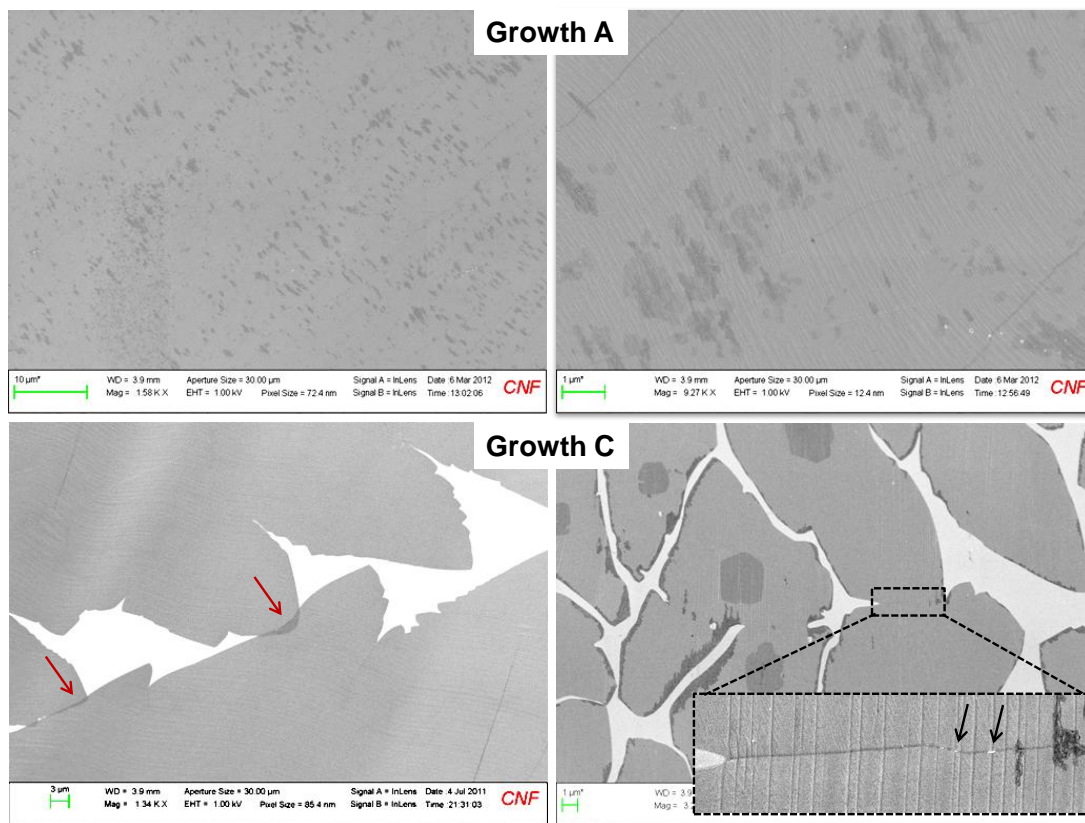
**Fig. S4**

Effective length  $|\lambda|$  as function of hole density  $n = C |V_G - V_{Dirac}|/e$  for devices shown in Fig. 2A, B, E.  $\lambda$  changes only within a factor of  $\approx 2$  as  $n$  is tuned by three orders of magnitude.



**Fig. S5**

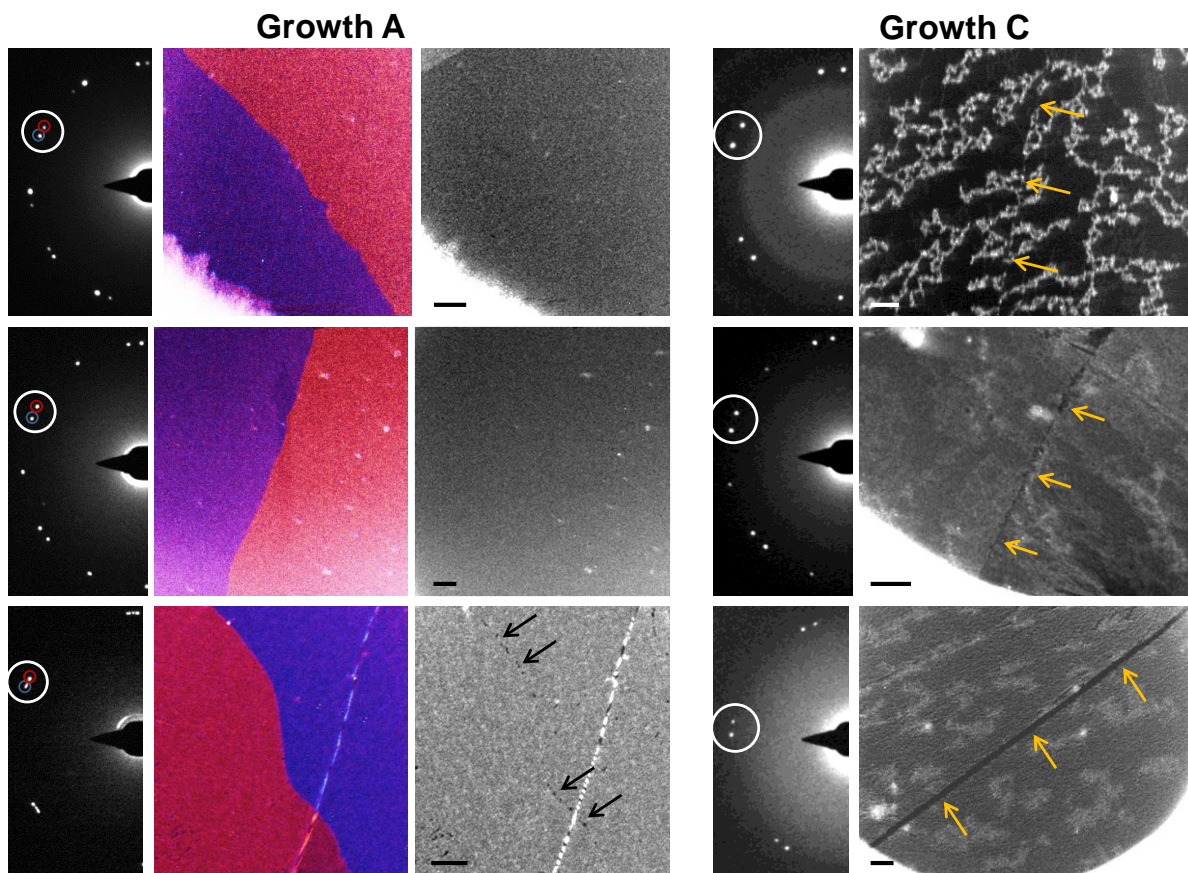
Intra-domain sheet resistance (L, R) measured at the Dirac point for all TEM-resolved devices. No strong differences are seen between growths A and C.



**Fig. S6**

Scanning electron micrographs of growths A (top) and C (bottom) on copper foil. Growth A completely covers copper surface, but growth C shows many areas with gaps and overlaps (denoted by red arrows), suggesting reduced tendency for inter-domain merging. Zoom-in image of area between islands shows dark line and small holes on boundary (denoted by black arrows).





**Fig. S7**

Dark-field TEM images of individual grain boundaries from growths A (left) and C (right) suspended on holes. Diffraction spots and apertures used to form images are shown in insets. Domains from growth A almost always make seamless connections when selecting both spots simultaneously, although dark spots (denoted by black arrows) indicate imperfect stitching occasionally. Boundaries from growth C (denoted by gold arrows) are always visible with varying amounts of discontinuity.

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